Network-on-Chip for a Partially Reconfigurable FPGA System

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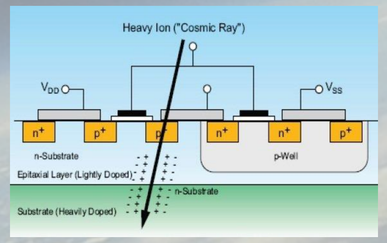
Abstract

A custom 1U CubeSat form-factor reconfigurable computing development platform has been designed and built for the purpose of implementing and testing multicore and multiprocessor systems. The platform was designed to leverage the active partial reconfiguration and configuration readback capabilities of the Xilinx Virtex-6 device. This enables myriad research opportunities in parallel processing, high-performance reconfigurable computing, and multicore/multiprocessor system design. An example application features a nine-processor radiation tolerant computer system which motivates further research into network-on-chip solutions for reducing multicore system routing complexity.

Radiation effects

Ionizing Radiation

- High-energy electrons
- High-energy protons
- Neutrons
- Heavy ions



http://spaceinimages.esa.int/Images/2012/12/Radiation-driven_Single_Event_Effect

Electronics Susceptibility

- Modern integrated circuit technology is susceptible to ionizing radiation.
- Radiation strikes leave a trail of electron-hole pairs in the silicon substrate of a device.
- Sufficient charge generation can result in state changes of bistable circuit elements.

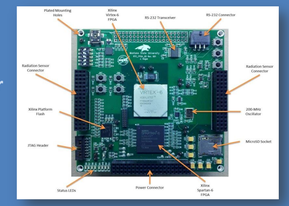
Single Event Effects (SEE)

- Single event transient (SET) – transient current induced by ionizing radiation
- Single event upset (SEU) – an erroneous transient that causes a circuit element state change
- Single event functional interrupt (SEFI) – an upset occurring in a circuit element which controls functionality of a device, such as an FPGA clock management tile or configuration controller.

FPGAs in space

Why use SRAM-based FPGAs?

- Performance – FPGAs enable hardware-accelerated processing and optimized IP cores
- Low power – modern design processes reduce power consumption
- Flexibility – in-system design changes, runtime hardware instantiation on an as-needed basis
- Low-cost – high-volume manufacturing lowers cost



Radiation Susceptibility

- Upsets can affect memory elements in the user design or in the device configuration memory
- Traditional fault mitigation techniques (e.g. TMR) handle faults in the user design
- Configuration memory faults must be detected and mitigated separately

FPGA systems require comprehensive fault mitigation strategies for aerospace applications

Our approach – Circuit-level fault mitigation

Fault Detection

- Readback scrubbing detects bit errors in configuration memory
- Traditional TMR detects and mitigates faults in the user design

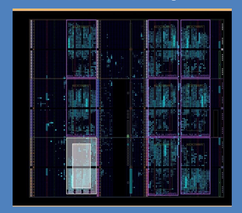
Redundant Many-Tile

- Coarse-grained triple modular redundancy (TMR) + voter
- 9 computational tiles for active triad + spares
- Spare tile health maintained in background using active partial reconfiguration

Recovery

- Replacement of faulted tile with healthy spare
- Faulted tile repair via active partial reconfiguration

9-tile Microblaze FPGA design



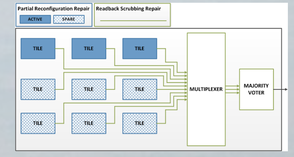
Our approach – Interconnect fault mitigation

Motivation for network-on-chip

- Centralized voter circuit represents a single point of failure
- Lack of inter-tile communication limits system performance and flexibility
- Tile faults and routing-related faults are indistinguishable

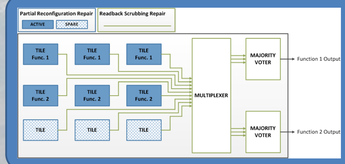
Single function system

- Centralized majority voter circuit
- Active-tile routing to voter through a multiplexer
- Dedicated tile-to-voter routing scheme
- No inter-tile communication



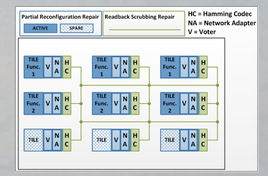
Multi-function system

- Multiple active TMR systems
- One voter circuit per system function
- No inter-tile communication
- Multiplexer routes active tile signals to their respective voter circuits



Shared Interconnect

- Decentralized voter - each tile contains a voter circuit
- Network adapter handles bus access
- Hamming Codec protects data and distinguishes routing and tile faults

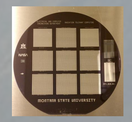
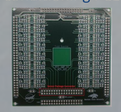
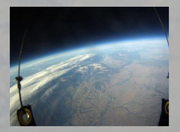
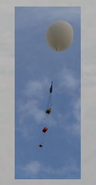


Hamming code

- Data is encoded immediately upon leaving a tile
- Hamming code mitigates single bit routing faults
- Voter circuits compare data and Hamming codes from each tile
- Fault recovery is based on fault location

Case	Selected Shared Network Fault Scenarios				
	Self-assessment	External Tiles	Hamming Code	Repair Technique	Fault Description
1	GOOD	GOOD	GOOD	N/A	Nominal Operation
2	GOOD	BAD	GOOD	PR	External. tile fault
3	GOOD	BAD	BAD	SCRUB	Routing fault
4	BAD	GOOD	GOOD	PR	Internal tile fault

Research Timeline

- Early computer system on development boards 
- Radiation sensor test circuit 
- Radiation sensor wafer 
- Packaged radiation sensor 
- Sensor signal conditioning PCB 
- Integrated sensor/FPGA development system 
- 1st & 2nd sounding balloon flights (~90k ft) MSGC BOREALIS 
- 1st & 2nd radiation tests at Texas A&M cyclotron facility 
- 3rd & 4th sounding balloon flights (~90k ft) MSGC BOREALIS 
- RockOn sounding rocket training program 
- Custom research hardware finished 
- 5th sounding balloon flight (~120k ft) NASA/LSU HASP 
- 3rd radiation test at Texas A&M cyclotron facility 
- 6th & 7th sounding balloon flights (~90k ft) MSGC BOREALIS 
- 8th sounding balloon flight (~120k ft) NASA/LSU HASP 
- 1st suborbital rocket flight ~100 mi.. 

2010 — 2011 — 2012 — 2013 — 2014