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Logic Analyzer Probing Techniques for High-Speed Digital Systems

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Abstract

Digital systems are turning out designs with faster edge speeds, double data rate clocking, and differential signaling to enable such systems to run faster than before. Adopting these techniques requires new considerations in circuit design, board layout, and system validation. Signal integrity is a term used to describe the quality of the signals in the system. If careful consideration is not given to the quality of the signals in the system, the design may fail to function properly. Signal integrity is emerging in the vocabulary of digital designers, a main focus of the definition, design, and debug of circuits and pc boards.

Many digital systems rely on logic analysis as part of the system validation plans. When probing high-speed digital signals with a logic analyzer, the designer must take the electrical characteristics of the probe into consideration. Designers are learning that not only do the electrical characteristics of the probe matter, but also the electrical characteristics of the methods used to connect to the probe. The connection to the probe is part of the circuit. The connection to the circuit is part of the probe. The design must account for probing *and* techniques when evaluating the effect of logic analyzer probing on the system's signal integrity.

With a variety of probes to choose from, the designer needs to consider not only which probe to use, but also how to connect to that probe. In many cases, answering the "how to connect" question is much more important than "which probe to use". Both the "how to" and the "which probe" questions need to be addressed when choosing a logic analyzer probing solution. This paper will discuss the pros and cons of several solutions of connecting a logic analyzer probe to a target circuit. Much of the analysis applies to both single-ended and differential signaling. However, differential signaling poses unique challenges, requiring additional consideration.

The analysis in this paper demonstrates the effect on signal integrity for several different probing solutions. All probing solutions will have some effect on signal integrity. The analysis of the solution provides readers with some practical rules-of-thumb and guidelines for determining which solutions minimize the effect on signal integrity.

Author(s) Biography

Brock J. LaMeres received his BSEE from Montana State University in 1998 and his MSEE from the University of Colorado in 2001. He is currently a hardware design engineer for Agilent Technologies in Colorado Springs, CO where he designs logic analyzer probes. He is also a part-time instructor at the University of Colorado in Colorado Springs in the area of microprocessor systems. His research interests are modeling and characterization of transport systems and high-speed digital design.

I. Introduction

Verification of digital systems has and always will be a vital piece of the product development cycle. As speeds increase, it is becoming more and more important to incorporate testing ability into the initial design. With printed circuit board (PCB) speeds starting to enter into the Gb/s era, it is becoming increasingly challenging to make the target system operate, let alone consider the electrical parasitics of testability. This paper discusses the impact of adding logic analysis testability to PCB's. In addition, techniques are presented to successfully probe digital systems to minimize the effect on the user's system, while ensuring the logic analyzer still has enough signal integrity to operate. Finally, modern examples of logic analyzer probing solutions are presented and the advantages and disadvantages of each solution are discussed.

II. Why Use a Logic Analyzer?

A logic analyzer is a piece of digital test equipment that is used for verification at the system level (i.e., digital signals transmitted between components). A logic analyzer can probe 300+ signals simultaneously, determine the logic level at a specific time, and present the data to the user in a variety of ways. The most common methods of presentation are the waveform and listing. The logic analyzer can monitor the data for certain patterns and sequences and present the data around the desired event. The analyzer can acquire data synchronously by using the user's system clock. This method is referred to as STATE analysis. It can also acquire data using an internal, asynchronous free-running clock. This method is referred to as TIMING analysis. This method gives the user relative timing information between the signals. Modern logic analyzers also have an acquisition mode that provides signal integrity information (eye diagrams, setup and hold information, scope display, etc…).

The obvious advantage of a logic analyzer is the signal count. A typical oscilloscope can observe up to 4 channels, while a logic analyzer can observe over 300. The other main advantage is that since the data is digital, it can be post-processed to provide information such as inverse assembly. In addition, complicated trigger sequences can be set up to observe the system during corner-case operation. State machines can be exercised under all conditions and the logic analyzer will be able to recognize the condition of the state machine and display the data only around a pre-defined event. Finally, once a system is probed, all three modes of analysis can be used (STATE, TIMING, and Signal Integrity). An oscilloscope is still the test equipment of choice if the true analog behavior of an individual signal needs to be observed while the logic analyzer provides validation at the multi-signal system level.

III. Probing Effect on the System

The inherent goal of probing is that the probe does not present a noticeable load on the target system. At lower frequencies, the effect of a logic analyzer probe on the target system is negligible. But as frequencies increase and the target system as well as the logic analyzer are operating at full speed, considerations must be made to ensure the testability is successful.

The most important concept that must be realized in logic analyzer probing is that the probe is part of the circuit. The probe will act as a load on the target system, both AC and DC wise. Obviously the main goal of a logic analyzer probe is to alter the target signals as little as possible. The second major

consideration that must be made is that the analyzer has minimum requirements to operate. These include sufficient bandwidth, minimum pulse-width, minimum voltage swing, etc…

Also important is the location of the probe on the target transmission line. The three main choices for the probe are at the source, midbus, and at the load. Depending on the termination method used on the target, each of these probe locations will have different effects on the user's system. Since the probe is an impedance, it will cause rise-time roll off and reflections in the system. Examples of the effect of probing location are given in section VI.

Another popular and often unintentional method of probing is known as stub-probing. This is where there is a length of trace between the probe tip and the target signal. This causes additional capacitive loading on the target in addition to rolling off the bandwidth of the signal that the analyzer sees. Specific examples of this methodology are presented in sections VII and VIII.

IV. Logic Analyzer Requirements

An important consideration for successful probing is the signal fidelity going into the logic analyzer probe. The first specification that must be met is the minimum signal swing. This is a specification that the logic analyzer vendor gives that states the minimum voltage swing that the target can have and still be detected by the logic analyzer probe. Modern probes can detect on the order of 250mV$_{pp}$. This can be a problem when a double-termination scheme is used. The nature of this termination scheme will divide the signal amplitude by two. The signal may be inadvertently too small for the analyzer to detect. For example, if the driver is producing 400 mV down a transmission line that is double-terminated, the actual voltage swing will be 200mV and will not meet the minimum voltage spec for the logic analyzer.

Other specifications that must be considered are the minimum pulse width, minimum setup/hold time, and maximum frequency. Since a logic analyzer is a digital comparitor device, it determines the logic level based on a pre-defined voltage threshold. Signal Integrity issues such as reflections and cross-talk may cause the logic analyzer to see a transition and must be considered.

Supplying the necessary bandwidth to the probe is also a consideration. For example, if stub-probing is used, the stub acts like a capacitance on the target signal. If the stub is long enough, it can roll-off the risetime so that the signal at the analyzer is not sufficient to determine a logic level. As frequencies increase, all of these considerations must be made. Section VIII gives examples these cases.

V. Load Model of the Logic Analyzer Probe

Now that the general ideas of logic analyzer probing have been discussed, we can look at how to predict the effect on the user's system when adding a logic analyzer probe. The most accurate way to predict the performance of a probed system is to include a probe load model in the system simulations. Logic analyzer vendors provide RLC circuits that model their probe loads up to a pre-defined frequency (usually 6 GHz). Simulations not only provide the most accurate model of the probe's effect, they provide a way to alter variables and monitor each variable's effect. These variables include probe location on the transmission line, and/or probe stub length from the transmission line to the probe tip.

In general, a logic analyzer probe will look as follows:

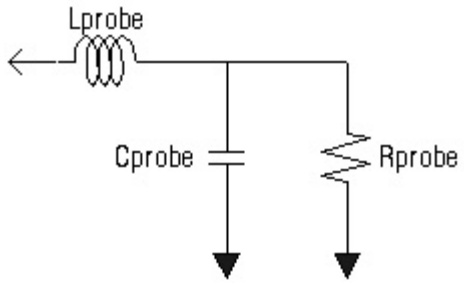


Figure 1. Simplified Load Model of a Logic Analyzer Probe

An important property of a logic analyzer probe is its impedance vs. frequency profile. This gives information to the user about when the impedance of the probe is on the same order of magnitude to the target transmission line impedance. This is important because if the probe impedance becomes too low, it will begin to look like an impedance divider and cause large reflections.

At lower frequencies, the resistor will dominate the probe's impedance and will have minimal effect on the target. This is because the probe impedance is on the order of 20k Ω's and the target is typically 50 – 75 Ω's. The two impedances are in parallel and yield most nearly the target impedance. As the frequency goes up, the probe will begin to look capacitive and its impedance will start to roll off. Once the impedance gets on the order of magnitude of the target impedance, reflections from the probe become an important issue. The following example illustrates the important of the impedance response of the probe.

> Example:
>
> A 50 Ω transmission line will experience a –10% reflection when it sees a load of 41Ω's. 41Ω's corresponds to an impedance of 228Ω's in parallel with the 50Ω transmission line. The frequency at which the probe impedance drops to 228Ω's will cause a –10% reflection of that frequency component.
>
> For a 75 Ω transmission line, the –10% reflection will occur on the frequency component where the probe impedance reaches 338Ω's.

At very high frequencies, the probe looks inductive and the impedance will increase. The capacitive and inductive nature of the probe load forms a resonance. The goal of the logic analysis probe is to push its resonance as far up in frequency as possible. In addition, the impedance at resonance should be as high as possible. If the probe impedance gets down in the range of 10-20Ω's, the probe will shunt out the higher frequency components of the target system. Figure 2 shows the equivalent model of the E5378A, 34 Channel, Single-Ended Probe from Agilent Technologies, Inc. Notice the resistive, capacitive, and inductive components of this model.

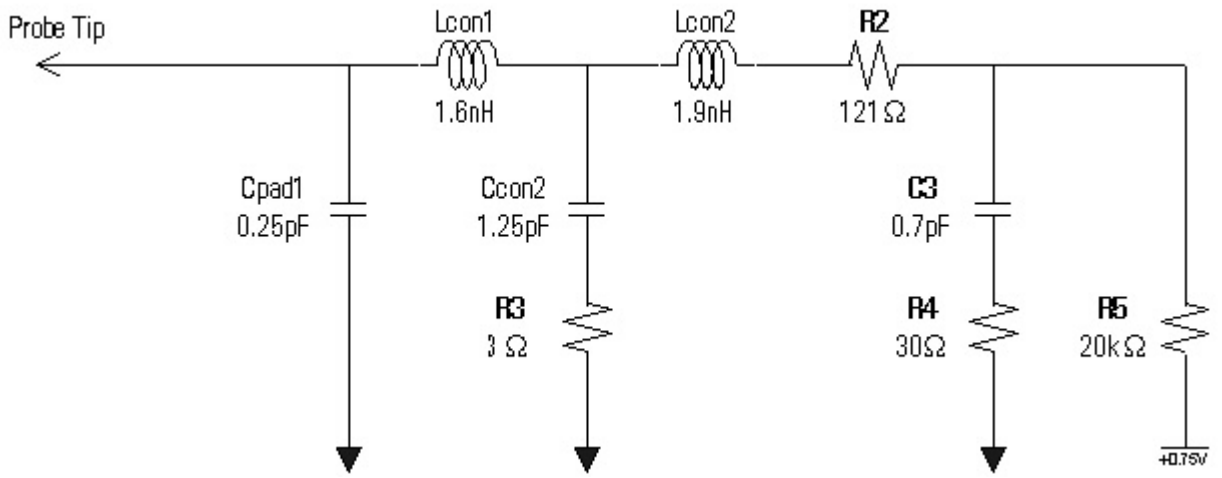
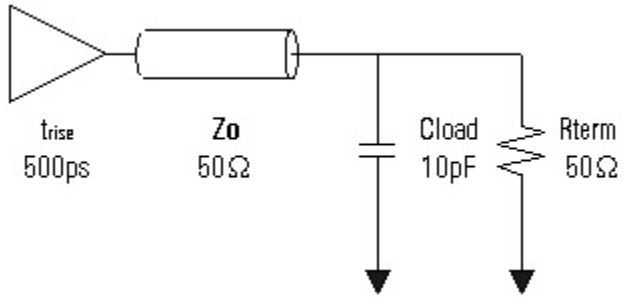


Figure 2. Equivalent Load Model of the E5378A Logic Analyzer Probe

As discussed, simulating the load model is the most accurate method of determining its effect on the system and is always recommended. It is sometimes useful though to have a quick way to estimate the probe load's effect on the target. For a quick estimate, using the equivalent capacitance will give a first order approximation of the probe's effect. This technique assumes the DC resistance is infinite and the probe has no inductance. Figures 3, 4, and 5 shows examples of how the total capacitance can be used to make a quick estimate on system performance. These examples use the total capacitance from the E5378A probe discussed earlier which is given by the manufacturer as 1.5pF.

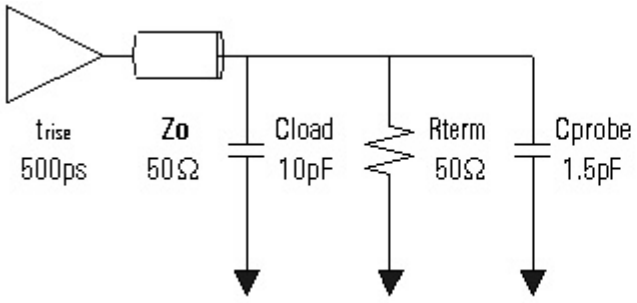


$$\tau_{load} = R \cdot C = (50 // 50) \cdot (10p) = 250ps$$

$$t_{riseload} = 2.2 \cdot \tau_{load} = 550ps$$

$$t_{risesys} = \sqrt{(500ps)^2 + (550ps)^2} = 743ps$$

Figure 3. System Risetime without Probe



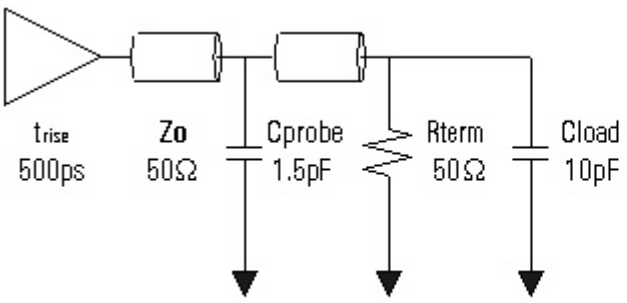
$$\tau_{load} = R \cdot C = (50 // 50) \cdot (11.5p) = 288ps$$

$$t_{riseload} = 2.2 \cdot \tau_{load} = 632ps$$

$$t_{risesys} = \sqrt{(500ps)^2 + (632ps)^2} = 806ps$$

$$\%_{RisetimeRdl-off} = 8.5\%$$

Figure 4. System Risetime with Probe at Load



$$t_{risdload} = 550ps$$

$$\tau_{probe} = R \cdot C = (50 // 50) \cdot (1.5p) = 38ps$$

$$t_{risdprobe} = 2.2 \cdot \tau_{probe} = 83ps$$

$$t_{risdsys} = \sqrt{(500ps)^2 + (550ps)^2 + (83ps)^2} = 748ps$$

$$\%_{RisetimeRdl-off} = 0.7\%$$

Figure 5. System Risetime with Probe in the Middle of the Transmission Line (Midbus)

Another interesting characteristic of an analyzer probe is its impedance profile. The effect of a logic analyzer probe on a target is characterized by performing multiple high-frequency measurements. These measurements include Voltage Network Analyzer (VNA), Time Domain Reflectometry (TDR), and Time Domain Transmission (TDT). These measurements are taken on a near perfect 50 Ω system that is double-terminated. Using a near perfect system isolates the effect of the probe from the effect of the test fixture. A logic analyzer vendor will create an RLC model (shown in figure 2) that accurately models the measurements. The RLC model can then be used in simulations as an accurate representation of the probe. Figure 6 shows the impedance response of the E5378A Logic Analyzer Probe from Agilent Technologies, Inc. Notice at low frequencies, the probe has a high impedance (20k Ω's). As the frequency increases, the impedance starts to roll off due to the capacitance of the probe. A resonance occurs at 3.4 GHz at which the impedance is 10 Ω's. Above the resonant frequency, the probe looks inductive and the impedance begins to increase.

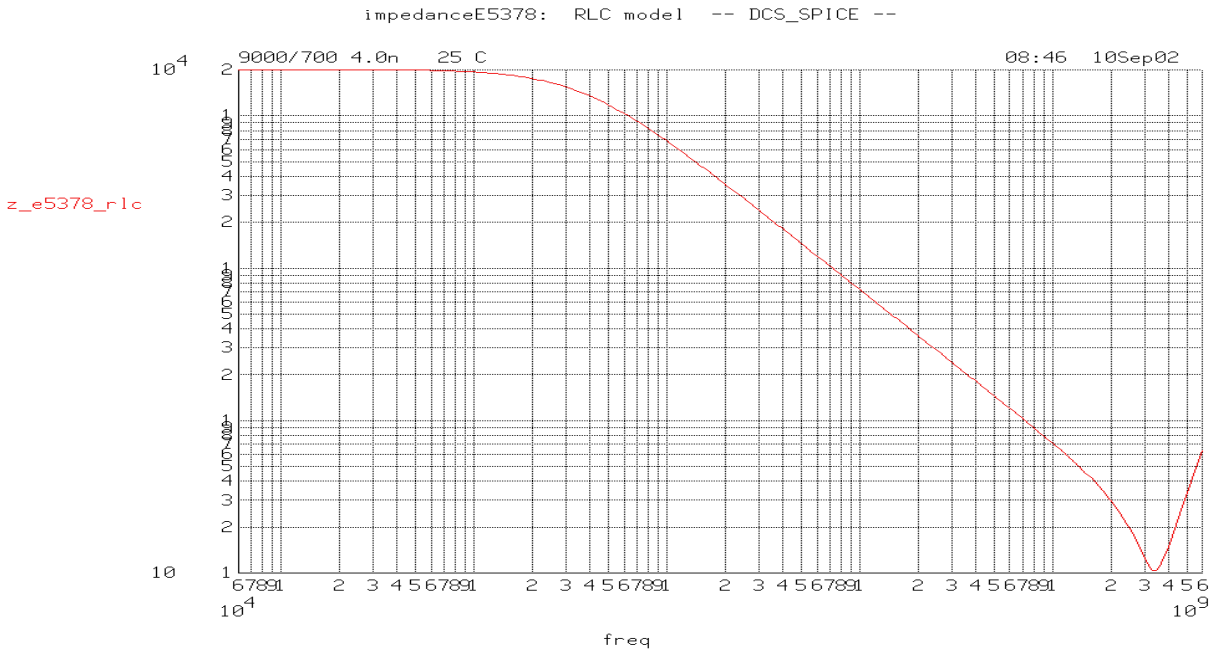


Figure 6. Impedance Response for the E5378A Logic Analyzer Probe

The impedance plot can tell the user information about reflections of certain frequency components. Again it is emphasized that the probe is part of the system and the topology of the transmission line is as important as the probe load. For example, large reflections may be tolerable on a double-terminated transmission line while small reflections may break a system that is poorly terminated. To get a feel for the transfer rate of a probe from its frequency response, a simple rule of thumb can be used.

transfer rate (b/s) = (probe resonant frequency (Hz) / 3) * 1.5

This equation sets the third harmonic of the maximum transfer frequency at the probe's resonant frequency. The fundamental of the transfer frequency is then found by dividing by 3. To find the transfer rate the number would traditionally be multiplied by 2. To give a small amount of margin, the number is only multiplied by 1.5.

Example:

The E5378A has a probe resonance of ~3GHz. Using the expression above:

transfer rate = (3 GHz / 3) * 1.5 = 1.5 Gb/s

VI. Probing Location Effect on Target

Since the probe is part of the circuit, its effects can be predicted. One of the major variables of the probe's impact is its location on the target's transmission line. The reflections that the probe causes will be determined by its relative position on the transmission line. Whether or not the reflections are of severe impact depends on the target system (i.e., trace length, termination scheme, voltage margin, etc…). In this section, examples of the effect of a logic analyzer probe are given. Two common termination schemes are presented, the load-terminated and the source-terminated topology. For each scheme, three probe locations are presented. The probe will be placed at the source, midbus, and at the load of the transmission line. These are the three most common probe locations.

For the first set of examples, the following circuit topology is used. Notice we are only concentrating on the load of the probe and not any load from the system. This is a 50 Ω, load-terminated system, with 4 inches of transmission line.

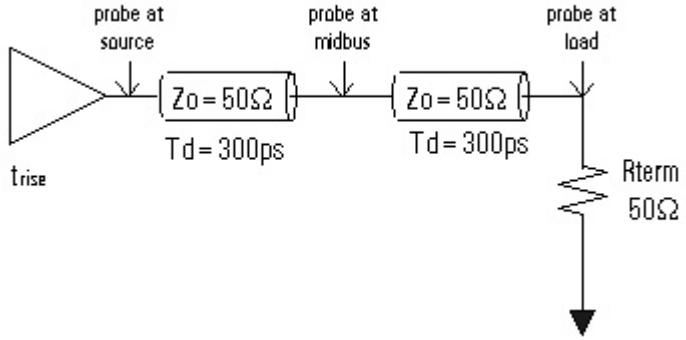


Figure 7. Circuit Topology for a Load-Terminated Transmission Line

The following three figures show the effect on the target signal at the load when the probe is located at each of the three locations, source, midbus, and load. For each probe location, 4 risetimes are presented. These figures clearly show that as the risetimes increase, the effect of the probe is more pronounced.

This is because higher frequency components are present in the system as the risetimes get faster. The higher frequency components will see lower probe impedance (see figure 6) and more severe reflections.

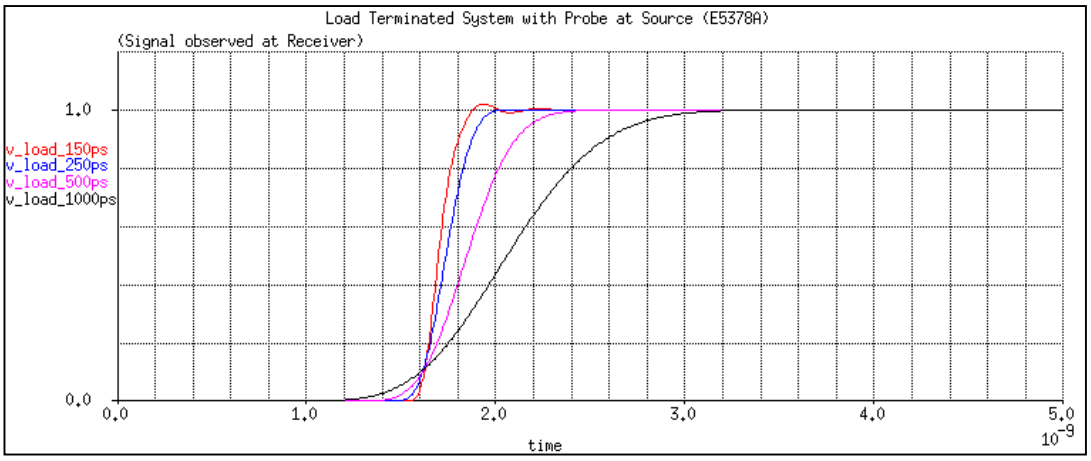


Figure 8. Effect on Load-Terminated System when Probed at Source

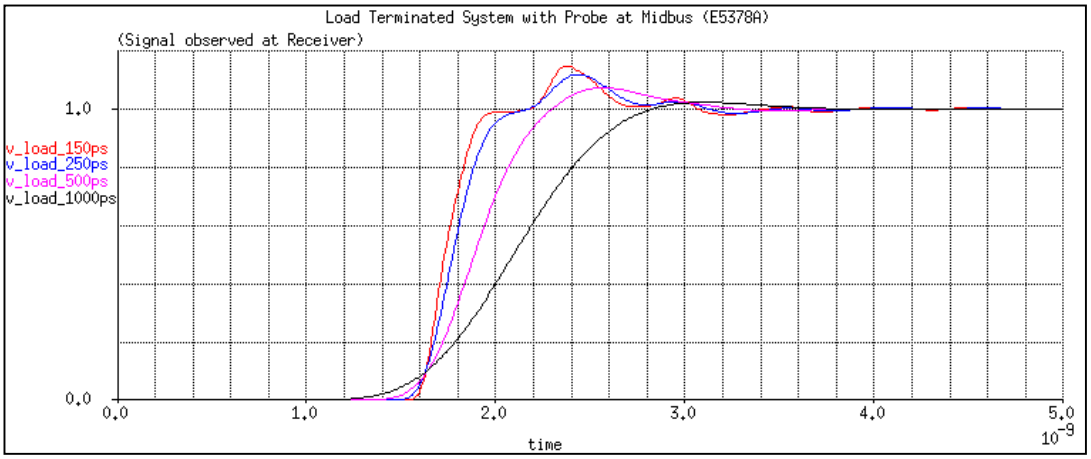


Figure 9. Effect on Load-Terminated System when Probed at Midbus

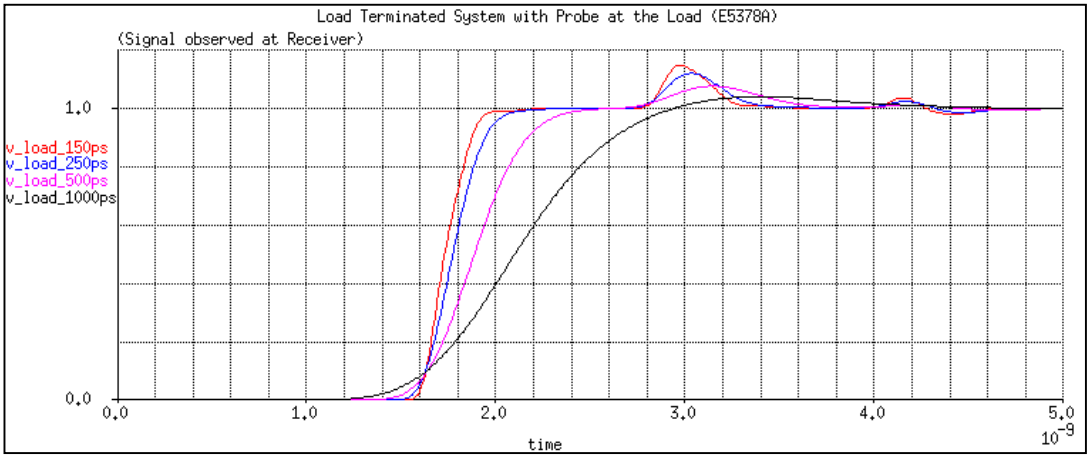


Figure 10. Effect on Load-Terminated System when Probed at Load

The next figures show the signal at the receiver of a source-terminated system. Again, three probe locations are presented. For each probe location, 4 risetimes are displayed.

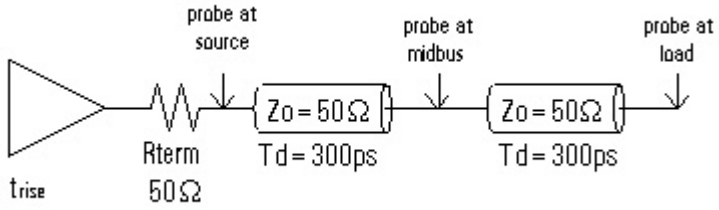


Figure 11. Circuit Topology for a Source-Terminated Transmission Line

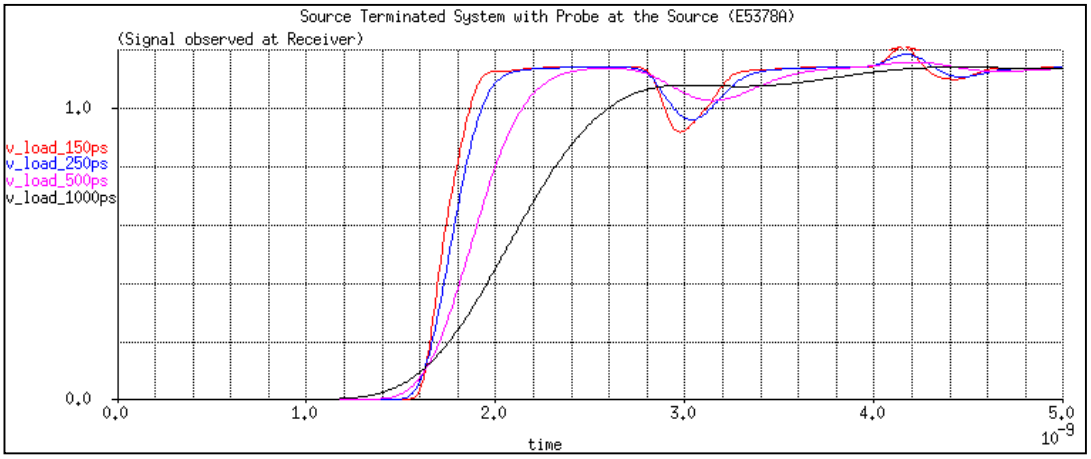


Figure 12. Effect on Source-Terminated System when Probed at Source

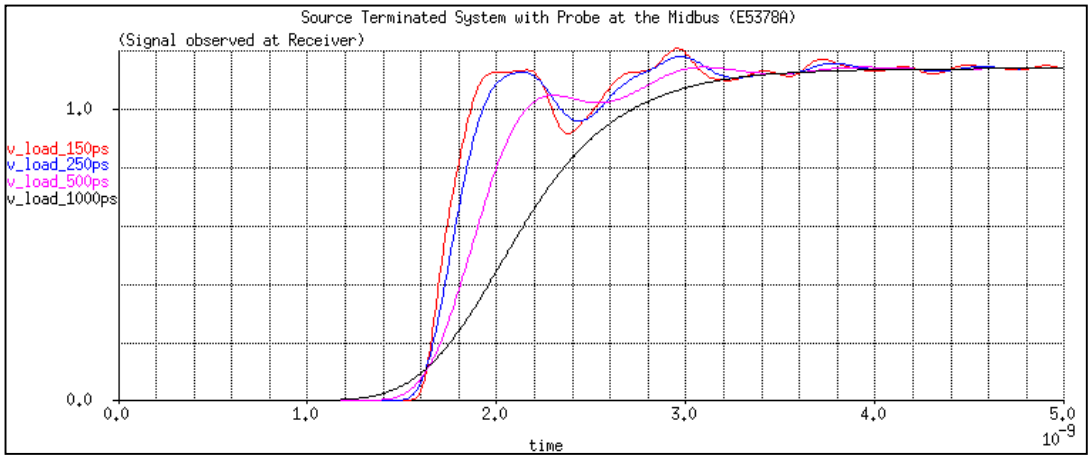


Figure 13. Effect on Source-Terminated System when Probed at Midbus

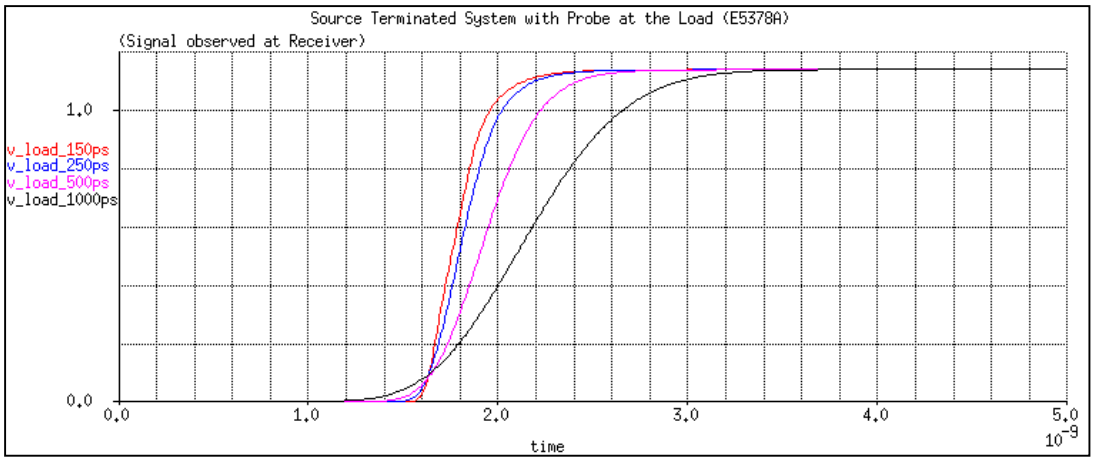


Figure 14. Effect on Source-Terminated System when Probed at Load

These figures demonstrate the importance of the probe location on the system performance. They also demonstrate how the effect of the probe is related to the risetime of the system. When estimating a probe's effect on a system, one of the first variables that must be considered is the system risetime. For risetimes on the order of 1000ps, the probe has little effect on the system independent of the probe location or termination scheme. However, for system risetimes of 150ps, the probe location and termination scheme make a major difference in the system performance.

These figures show the effect of only the probe load on the system. In a true system, there will be reflections caused by the load of the receiver (as well as other discontinuities). Figure 15 shows a comparison of the system in figures 3 and 4. This shows how a load-terminated system with a capacitive load of 10pF is effected by probing at the load. The two waveforms show the response with and without a probe. Only the 150ps risetime case is presented as it represents the worst-case performance. Clearly the reflections in the system are dominated by the 10pF load and the probe capacitance is a 2nd order effect.

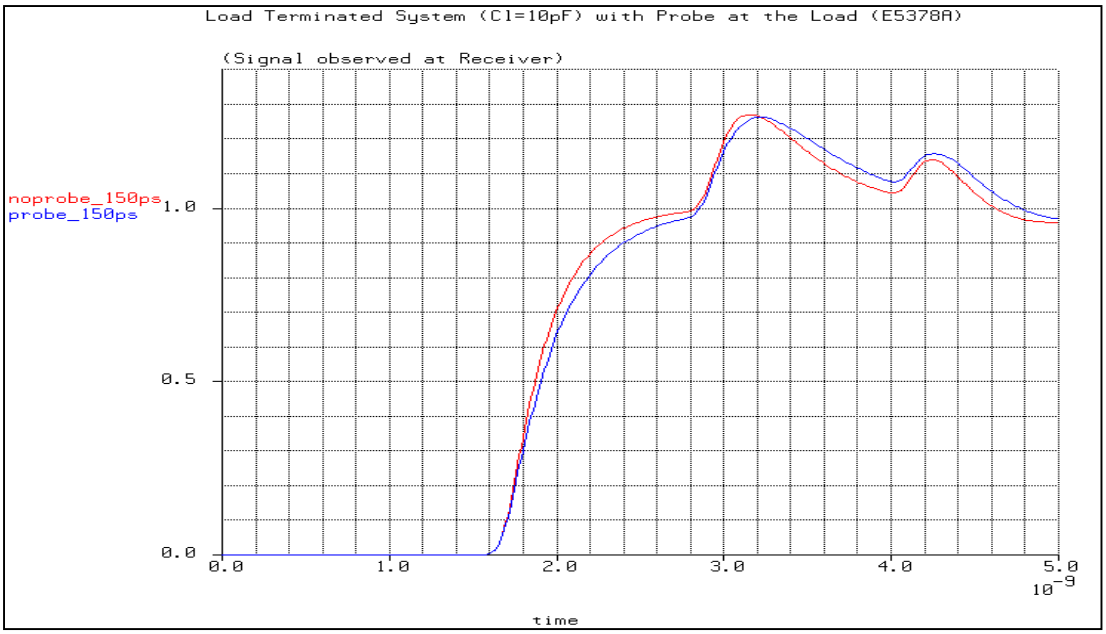


Figure 15. Effect on Load-Terminated System (C_{load}=10pF) when Probed at Load

VII. Probing Location Effect on Logic Analyzer

As mentioned earlier, the signal integrity of the logic analyzer must be considered to ensure successful probing. The previous section presented the effect of the logic analyzer probe on the targets signals. This section will present the effect of probing location on the signals that the probe sees.

Again, two common termination schemes are presented, the load-terminated and the source-terminated topology. For each scheme, three probe locations are presented. The probe will be placed at the source, midbus, and at the load of the transmission line. In these figures however, the signal is observed at the probe tip. For the next three figures, the load-terminated topology given in figure 7 is used.

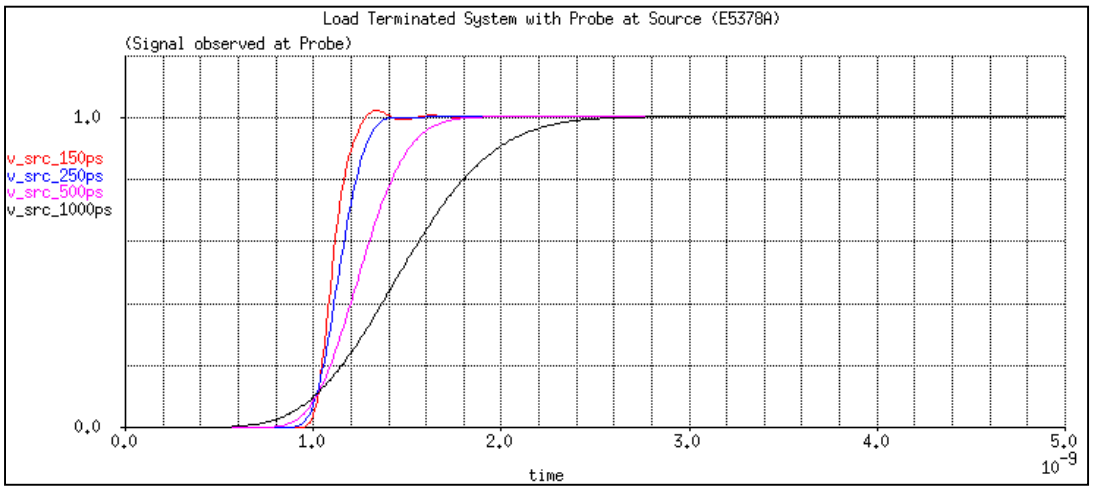


Figure 16. Signal at Probe of Load-Terminated System Probed at Source

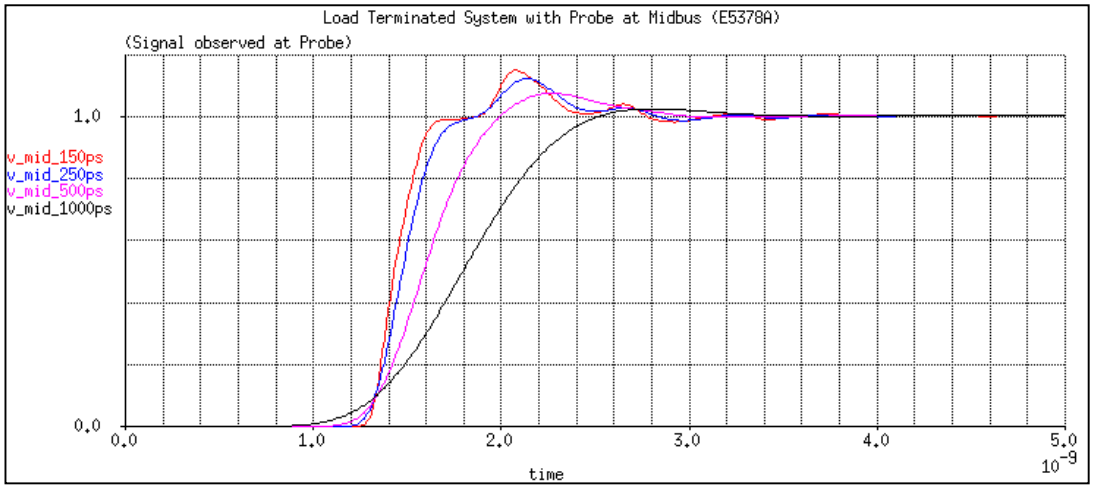


Figure 17. Signal at Probe of Load-Terminated System Probed at Midbus

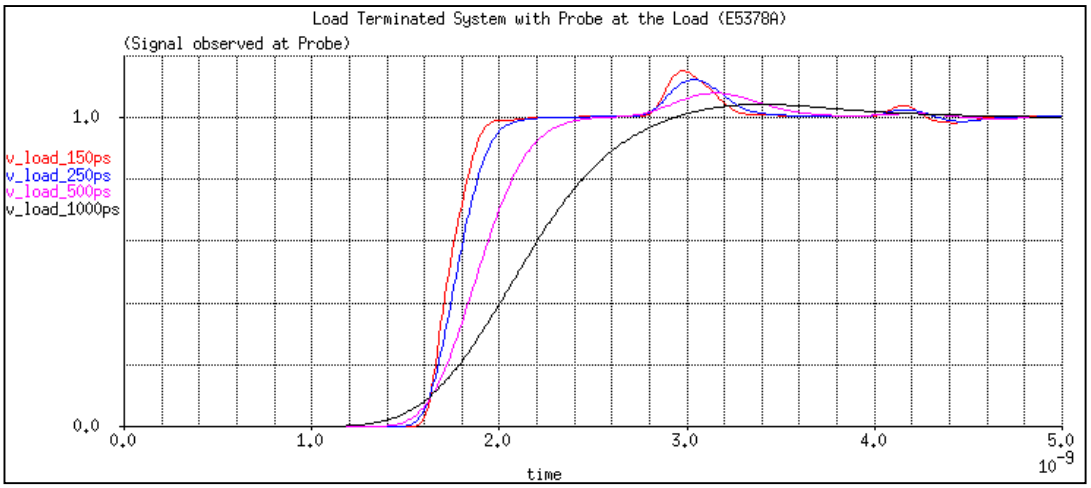


Figure 18. Signal at Probe of Load-Terminated System Probed at Load

These figures illustrate that the logic analyzer probe will see different signal quality depending on its location. The next set of figures show how probe location effects signal integrity for a source-terminated system. The topology for the source-termination scheme is show in figure 11.

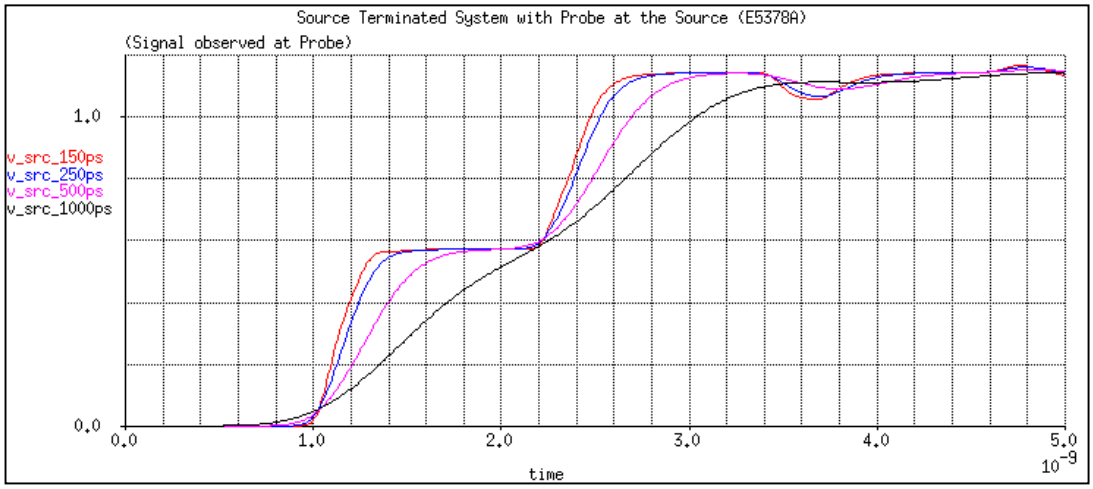


Figure 19. Signal at Probe of Source-Terminated System Probed at Source

Figure 19 shows that the analyzer will see a voltage that remains in the middle of the swing for up to 1ns. Since the analyzer determines the logic level by comparing the input signal to a voltage reference, there is no guarantee that the logic analyzer will be able to detect the correct level during this period of time. This is not an optimal point to probe a source-terminated system.

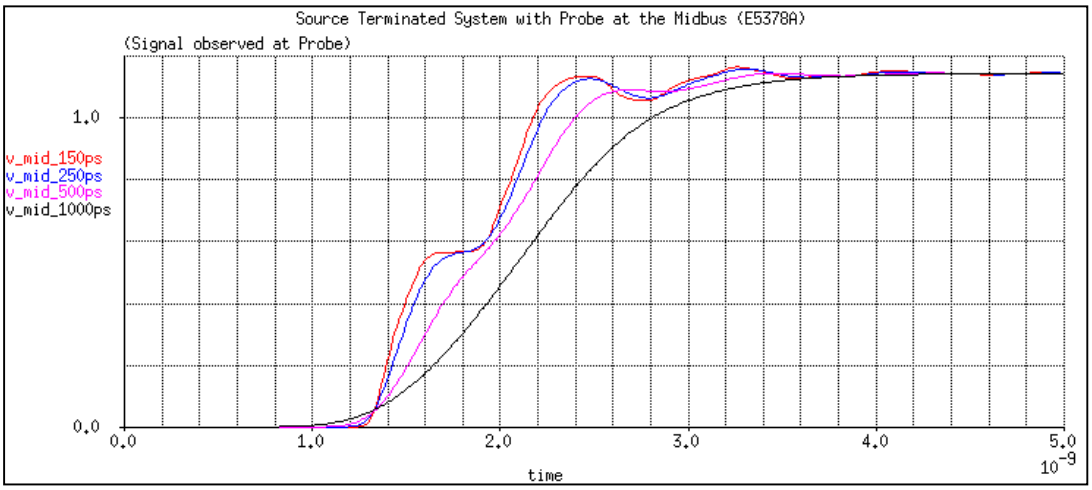


Figure 20. Signal at Probe of Source-Terminated System Probed at Midbus

This waveform again has a period of time where the logic level in indeterminate. Although this is not as bad as probing the source-terminated system directly at the source, it is still not the optimal probing location.

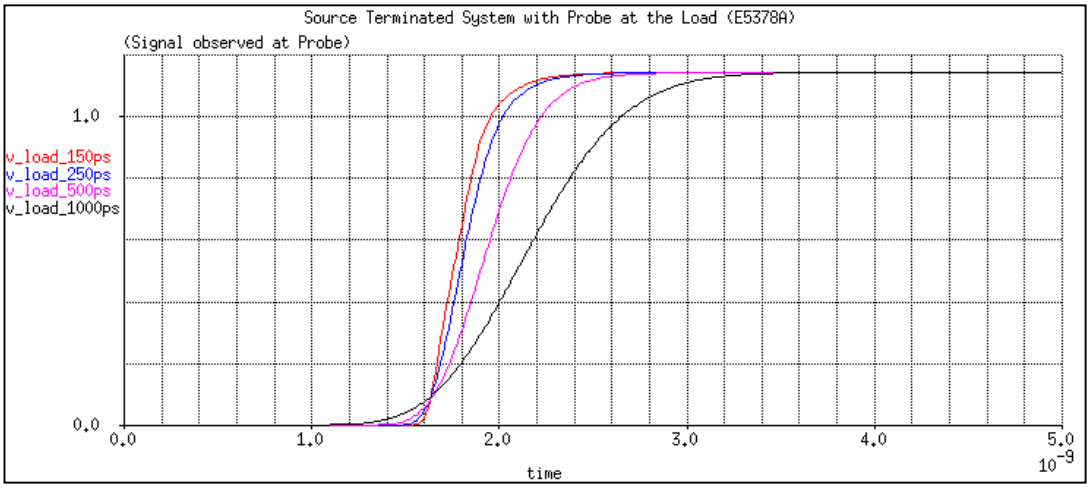


Figure 21. Signal at Probe of Source-Terminated System Probed at Load

This figure demonstrates that the most successful point at which to probe a source-terminated system is directly at the load. This ensures that the logic analyzer sees the full swing of the driver as it instantaneously reflects off of the high impedance receiver. At any point besides directly at the load, there will be a stair-step waveform that is intrinsic of the source-terminated system. This stair-step behavior is an unsuitable signal for the logic analyzer and should be avoided.

VIII. Stub-Probing

Stub probing refers to when the probe tip cannot be placed directly on the target's transmission line. The length of trace that runs between the probe tip and the target signal is called the stub. The stub can consist of PCB trace, wire, or the leads of a connector. Stub probing is difficult to avoid due to layout constraints on a PCB. The question then becomes how close does the probe tip need to be to the transmission line and still have acceptable performance in the system and in the logic analyzer?

When talking about transmission lines, the rules of thumb that are used are applicable to logic analyzer stubs. The rules of thumb depend on the system risetime. For a logic analyzer, the recommendation is that the stub have an electrical length of no more than 20% of the system risetime. For an electrical length that is less that 20% of the system risetime, the stub can be treated as a lumped capacitance and not a distributed transmission line. However, the capacitance increases greatly as the stub length increases. At a point, the trace capacitance will exceed the total capacitance of the probe. The following figure shows the stub-probe topology.

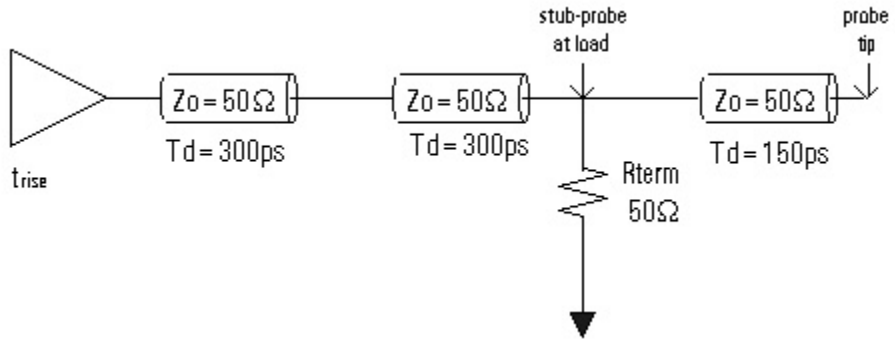


Figure 22. Load-Termination Topology with Stub-Probe at Load

The following example illustrates the maximum stub length acceptable for particular risetimes. This example uses a propagation velocity of 150ps/in, which is typical in FR4 dielectric PCBs. The unit capacitance is typically 3pF per inch for a standard 50 Ω, FR4 microstrip transmission line

Example:

Trise= 150ps,	Tstub=(150)*(0.2)= 30ps	Length=(30)/(150)=0.20"	Cstub=(0.2)*(3p)=0.6pF
Trise= 250ps,	Tstub=(250)*(0.2)= 50ps	Length=(50)/(150)=0.33"	Cstub=(0.33)*(3p)=1.0pF
Trise= 500ps,	Tstub=(500)*(0.2)= 100ps	Length=(100)/(1500)=0.67"	Cstub=(0.67)*(3p)=2.0 pF
Trise= 1000ps,	Tstub=(1000)*(0.2)= 200ps	Length=(200)/(150)=1.33"	Cstub=(1.33)*(3p)=4.0pF

If we look at a logic analyzer probe that is connected though a 1" stub to the load of a transmission line, we can illustrate the above example. Figure 23 shows the effect of a 1" stub-probe on a load-terminated transmission line when probe at the load. Four risetimes are again presented. The 150ps, 250ps, and 500ps risetimes consider the 1" stub to be unacceptable while the 1000ps risetime will operate properly. It is obvious from this figure that the 1000ps risetime has considerably better characteristics than the 150ps risetime.

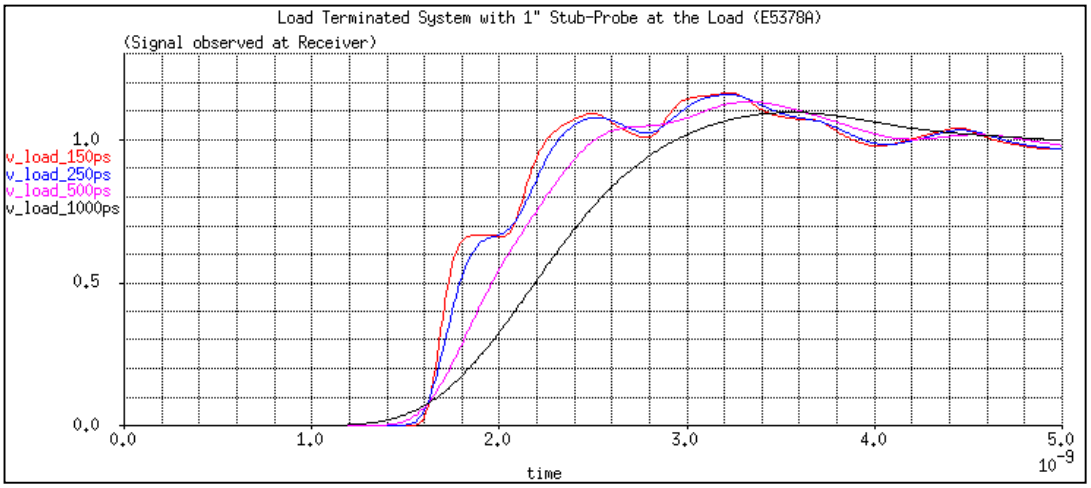


Figure 23. Signal at Receiver of Load-Terminated System with 1" Stub-Probe at Load

The next figure shows the signal at the probe tip for a 1" stub-probe. Again it is obvious that the 1000ps risetime has better characteristics than the 150ps risetime.

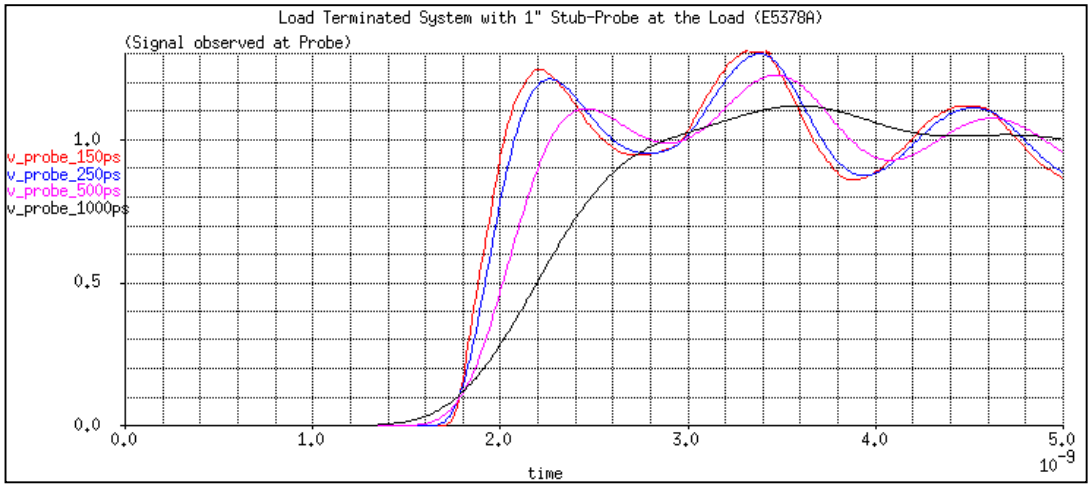


Figure 24. Signal at Probe Tip of Load-Terminated System with 1" Stub-Probe at Load

IX. Damped Resistor Probing

PCB constraints sometimes prevent the logic analyzer probe tip from being placed directly on the target transmission line. However, as risetimes increase, the stub length that is tolerable to the system becomes impractically short. One method that can increase performance when using stub-probing is to insert a damping resistor between the target signal and the stub going to the logic analyzer probe tip. A typical damping resistor is on the order of 125 Ω's. The resistor has two effects. First, it isolates the stub capacitance from the target transmission line. This has the effect of reducing reflections and improving the target risetime. The second effect is that the reflections that exist on the stub to the probe are dissipated in the resistor. This will reduce the ringing on the signal that the logic analyzer sees. The next figure shows the topology of the damped resistor probing scheme.

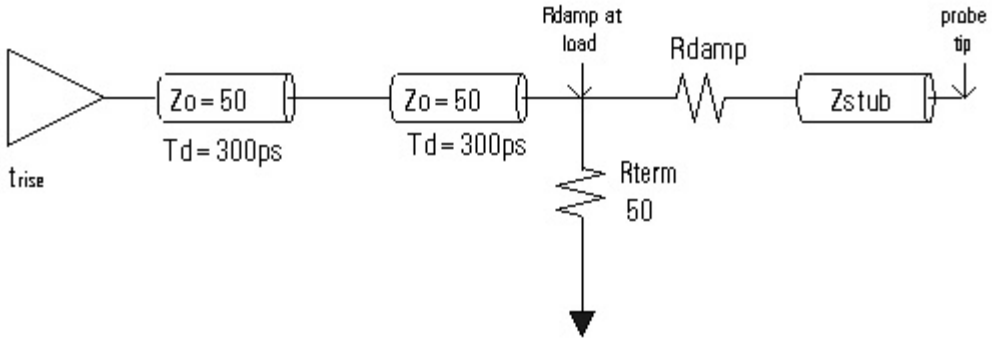


Figure 25. Load-Termination Topology with Damped Resistor Probe at Load

There are some considerations when selecting the value of the damping resistor. It is better for the target system if the resistor is large. However, the damping resistor forms an RC circuit with the stub capacitance going to the probe tip that will roll off the signal that the analyzer sees. So there is a balance to be struck between the system performance and the analyzer performance when using a damping resistor. The minimum critical value of the damping resistor is 25 Ω's. The maximum value of the resistor is going to be set by the RC circuit and the bandwidth needed by the analyzer. In general, selecting the damping resistor equal to 2½ times the impedance of the trace is optimal. The maximum stub length is then defined by the bandwidth needed by the analyzer.

Example:

Zo = 50 Ω's
Rdamp = 125 Ω's
Dstub = 1" (3pF)
Cprobe = 1.5pF
Rdrive = 125 Ω + (½ * Zo) = 150 Ω

Γ_{system} = [(125//50) – 50] / [(125//50) + 50] = -17%
$BW_{analyzer}$ = 1/(2πRC) = 1/(2π*150*4.5p) = 236 MHz = 472 Mb/s

This example shows that by isolating the capacitance of the stub, the reflection that the target will see due to the probe is reduced. It also shows that the bandwidth of the analyzer has been reduced due to the RC circuit formed by the damping resistor and the capacitance of the stub. 472 Mb/s is less than a 3rd of the rated specification of 1.5 Gb/s of the probe under ideal situations. A balance can be struck depending on the necessary performance of the system. A higher damping resistor is good for the target but reduces the bandwidth of the probe. The bandwidth of the probe can be increased by lowering the damping resistor value or by decreasing the length of the stub. One advantage of the damped resistor is that if the logic analyzer is no longer needed, the damping resistor can be removed and the load of the stub is removed from the system.

A modification of the damped resistor scheme is the resistive divider scheme. In this method, a load-termination resistor is placed at the end of the probe stub. This turns the stub into a terminated transmission line. In this configuration, the length of the stub no longer matters and much higher bandwidth is achieved. There are two things to consider when using this scheme. First, the signal amplitude that the analyzer probe tip sees will be reduced according to the divider ratio selected. This is an issue because if the signal is divided down below the minimum allowable voltage level of the analyzer, the signal may not be able to be detected. Second, the resistive divider will insert a DC load on the target system. Typically this load will be on the order of 200-400 Ω's. The driver must be able to withstand this DC load. The next figure shows the topology of the resistive divider probing scheme.

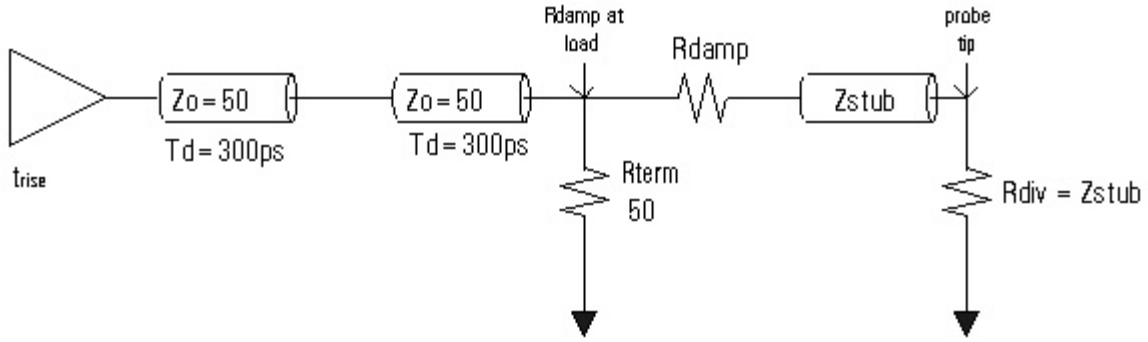


Figure 26. Load-Termination Topology with Resistive-Divider Probing Scheme at Load

The divider resistor is chosen to match the characteristic impedance of the stub and to set the divider ratio. Since the stub is now terminated, the impedance of the probe load will look purely resistive across all frequencies of interest. Now the considerations that must be made are selecting the divider ratio so not to violate the minimum voltage swing that the analyzer needs. Also, selecting the total resistive load on the target. The resistive load will still cause reflections in the system because it is an impedance in parallel with the target transmission line.

Example:

Zo = 50 Ω's
Rdamp = 125
Rdiv = 50
$V_{pp|target}$ = 1v

Γ_{system} = [(175//50) – 50] / [(175//50) + 50] = -12.5%
$BW_{analyzer}$ = full
$V_{pp|analyzer}$ = 1v * [50 / (125 + 50)] = 286 mV (meets spec)

It is desirable to choose the impedance of the stub to be as high as possible in order to get a larger signal swing at the analyzer and less reflections on the target. This will be limited by the constraints of the PCB stackup. In a PC5 process, it may not be possible to achieve a higher trace impedance without violating the design rules of the PCB manufacturer. If it is possible though, it is to the user's advantage.

X. Modern Probing Solutions

The mechanical considerations of a logic analyzer probe are just as important as the electrical ones. If the form factor of the probe does not easily integrate itself into the target system, then the probe is not useful. As discussed in previous sections, probe location makes a big difference to the signal integrity of the system and of the logic analyzer. The size and shape of the probe play a part in how close the probe tip can be placed to the target transmission line.

Logic analyzer probing solutions have evolved into three main categories:

1) Connector-Based
2) Flying Lead Based
3) Connector-Less

The connector-based probes are ones in which the user puts down a connector defined by the logic analyzer vendor on the target PCB. The signals of interest are routed to or through the connector. The logic analyzer probe will have the opposite sexed connected as its probe tip. The logic analyzer is then plugged into the target system. The E5378A from Agilent Technologies is an example of a connector based logic analyzer probe. This probe uses a 100 pin Samtec connector.

The next main category of logic analyzer probes is the Flying Lead. This connection method is more general purpose and provides the most flexibility to the user. The Flying Lead consists of individual wires around 6-12" in length. Each wire's end contains the probe tip of the logic analyzer. This method allows the user to probe many different regions of the board with one probe. This probing method is especially useful for signals that are not broken out to a connector in the initial design.

The final category of logic analyzer probes is called "Connector-Less" probing. This is the newest technology in logic analyzer probing and presents some of the most attractive options to the end user. The concept of a connector-less probe is that the user only puts down landing pads on his PCB. Traces are routed to or through the pads. A retention module is used to align the probe tip with the pads and provide mechanical stability. The logic analyzer probe is then attached to the board with the assistance of the retention module and makes contact with the pads on the board.

The advantages of connector-less probing are that since the signals do not travel through a connector to get to the logic analyzer probe tip, there is less capacitive loading on the target. For example, the E5378A probe discussed earlier had an equivalent lumped capacitance of 1.5pF. Connectorless probes are on the order of 0.7pF, a 2x improvement. Also attractive about this new technology is that the user does not need to load connectors onto the target PCB, reducing the cost of the final assembly. Finally, improvements have been made to the route-ability of connector-less probes. The user can now easily route directly through the probe pads without making layer changes. Since the capacitance is so low and there is no connector, the logic analyzer footprint can be left in the design on the final release of the PCB without any electrical degradation to system performance.

The next figure shows a picture of each of the three probing solutions previously described. On the left is the "E5378A, 34 Channel, Single-Ended Samtec probe". In the middle is the "E5382A, 17 Channel, Single-Ended Flying Lead probe". On the far right is the E5387A, 17 Channel, Differential Soft Touch (connector-less) probe. All of the probes shown are from Agilent Technologies, Inc.

Figure 27. Modern Probing Solutions
(Connector-Based, Flying Lead, and Connector-Less)

XI. Conclusion

This paper has presented techniques and considerations for logic analyzer probing. The equivalent circuit of a logic analyzer probe was discussed and its impact on the target system was examined. Estimating techniques were presented to get an initial feel for the impact of the probe on the system's performance. Probe location was examined as a variable in the performance of the system as well as of the logic analyzer signal quality. Examples of common termination schemes and common probing locations were given. In addition, methodologies and rules of thumb were presented for stub-probing, damped-resistor probing, and resistive-divider probing. Finally, the categories of modern probing solutions were discussed (connector-based, flying lead, and connector-less).

As PCB speeds get faster, testability becomes more important to the success of the project and to the time-to-market of a product. Logic Analysis is a testability method that lends itself well to prototype verification at the system level. With sub-nanosecond risetimes becoming the industry standard, any loading on the target system becomes crucial. When logic analyzer testability is selected, the effect of the probing contact must be considered in the initial stages of the design, both electrically and mechanically. At high speeds, the logic analyzer probe can no longer be thought of as a separate entity but must be included as part of the circuit. Simulating the load model is the most accurate method of determining the effect of the probe on the system performance. However, quick estimates can be made to determine the effect of the probe using the total capacitance of the probe or the probe's impedance profile. As important as the signal integrity of the system is the signal integrity of the probe. The same variables that affect the system performance, (probe location, termination scheme, and risetimes) affect the signal integrity of the signal that the logic analyzer probes sees. These issues must be consciously addressed in order to ensure successful system and logic analyzer operation.