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Dynamic Reconfigurable Computing Architecture for Aerospace Applications

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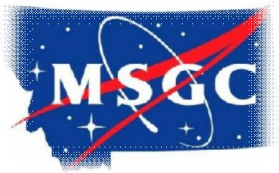
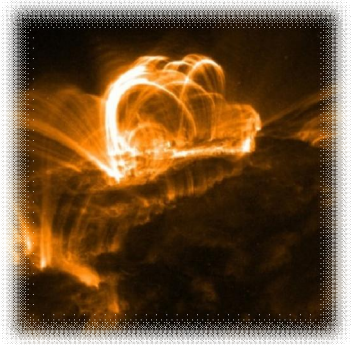


Motivation

Radiation-Hardness for Aerospace Systems



- Cosmic radiation induces transients in integrated circuits
- Commercial processes are susceptible to Singe-Event-Upsets (SEUs)
- Aerospace systems must address this additional constraint

Mitigation Techniques

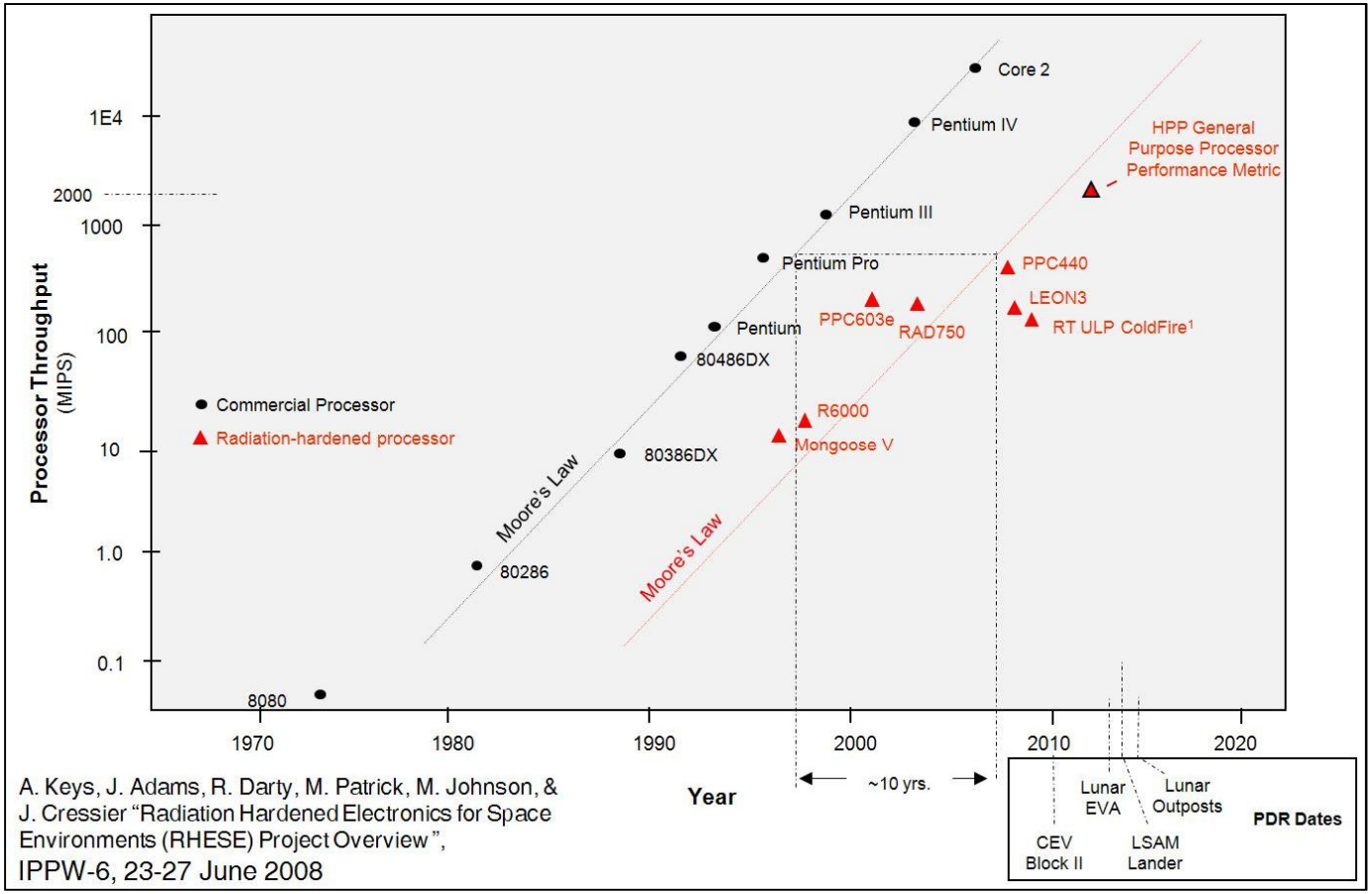
- A variety of approaches are used to achieve radiation-hardness:

1) Radiation by Architecture
   - *Triple Modulo Redundancy, Fault Recovery Processes, COP*

2) Radiation by Design/Process
   - *Substrate doping, Enclosed Layout Transistors, isolation trenches*

Motivation

The Drawback of Rad-Hard Processors

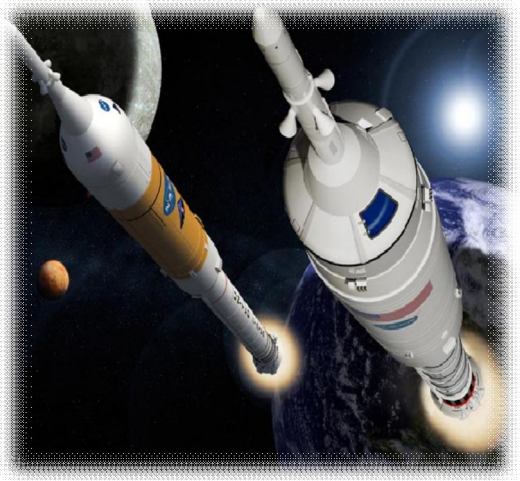


Radiation-Hardness translates into slower performance and more power consumption

Motivation

Programmable Logic

- Advances in programmable logic fabrication (specifically FPGAs) has enabled new solutions to the needs of the Aerospace industry



Opportunities for FPGAs in Aerospace

1) Radiation Hardness through TMR
   - *Designers can easily add as much or as little redundancy as needed*

2) Performance through multi-processors
   - *Easy to add parallel processing until design performance is achieved*

3) Reduction in Flight Spares
   - *Common platforms can be used for multiple systems*
   - *This allows a common replacement platform which means less spare mass*

4) Dynamic Reconfiguration
   - *Real time configuration can be used to optimized for the current application*

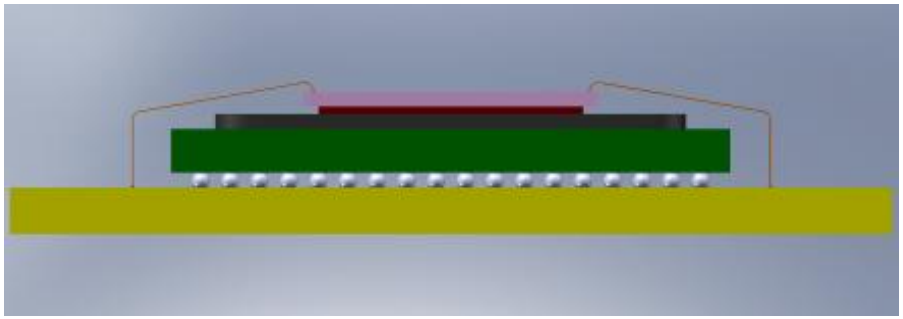
Our Approach

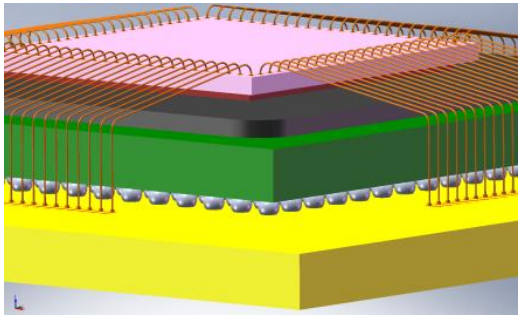
Dynamic Reconfiguration Based on Radiation Environment

1) A system that uses information about whether radiation is present or not
   - *Implemented on an FPGA allows the system to reconfigure based on its environment*

2) An SEU radiation sensor integrated with the FPGA
   - *Silicon based, double-sided strip detector feasibility has been demonstrated for nuclear physics*

3) System Optimization in Real-Time
   - *FPGA can reconfigure to achieve different performance objectives based on environment*
   - *"Radiation Tolerant" - TMR added if necessary*
   - *"High Performance" – parallel processing added as necessary*
   - *"Low Power" – hardware minimized if necessary*





System Design

Prototype Hardware

1) We have evaluated this technique using a Xilinx Virtex-5 Eval Platform (ML507)

2) A simple peripheral controller application was used
   - *Reading PS2 keyboard and writing to an LCD*

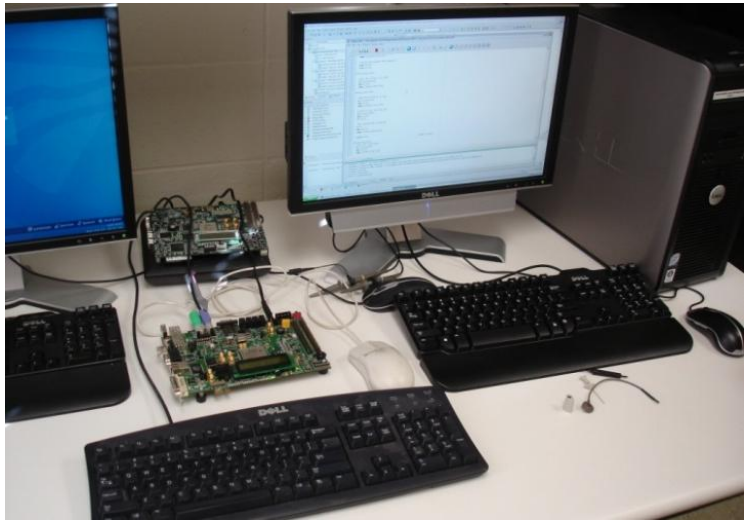
3) The picoBlaze soft processing core was used to accomplish the computing task

4) Dynamic reconfiguration accomplished using SystemACE

System Design

Modes of Operation

- Mode 1: Parallel Processing
- Mode 2: Low Power
- Mode 3: Radiation Tolerant



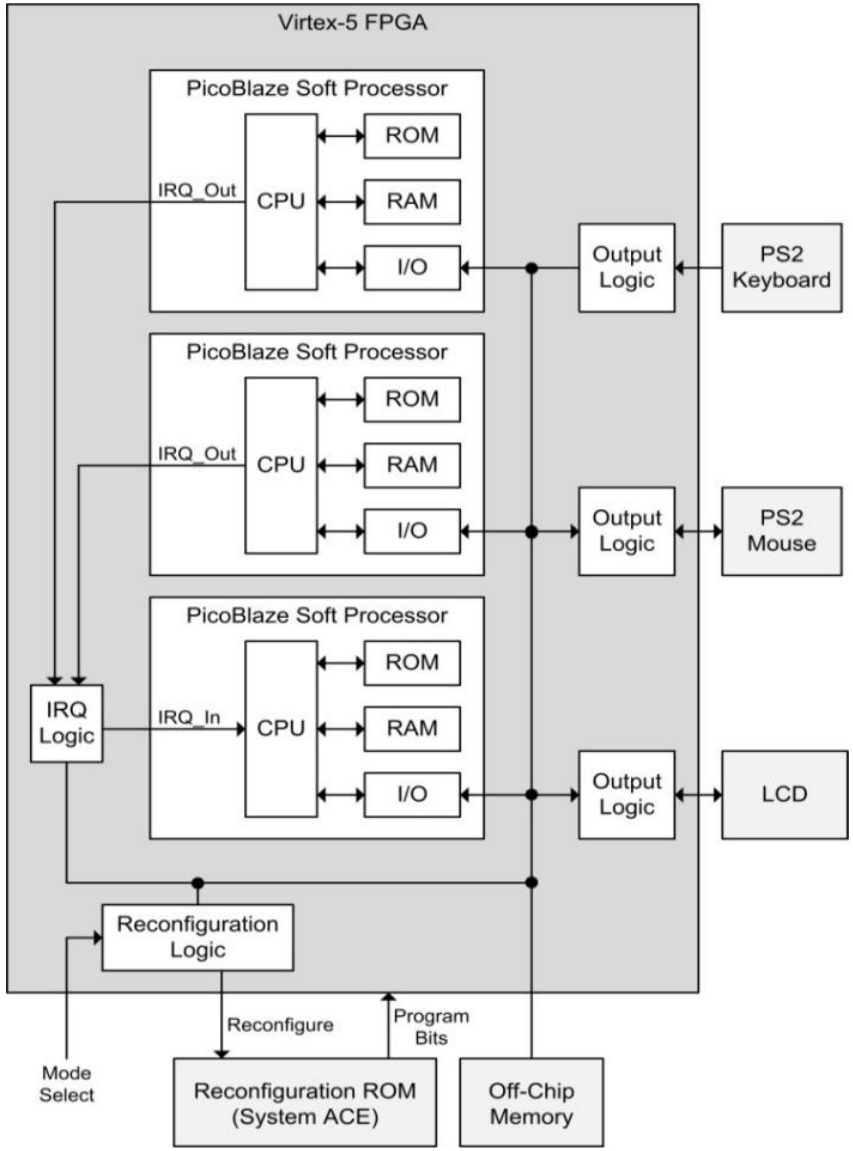
1) Parallel Processing Mode

- If **No Radiation** is present

  - the FPGA can be configured with multiple processors to increase performance

  - each processor is assigned a specific task and has different code-lines

  - each processors has routine for reconfiguration based on signal from external radiation sensor

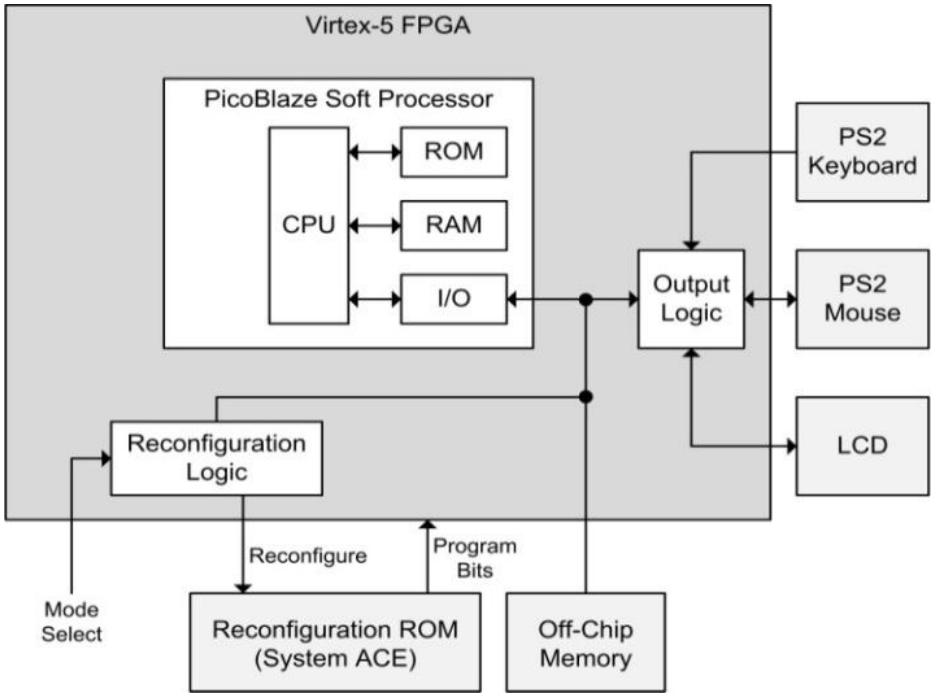


2) Low Power Mode

- If **No Radiation** is present

  - the FPGA can be configured with a single processor that accomplishes each task in a sequential manner

  - The processor has a routine for reconfiguration based on signal from external radiation sensor



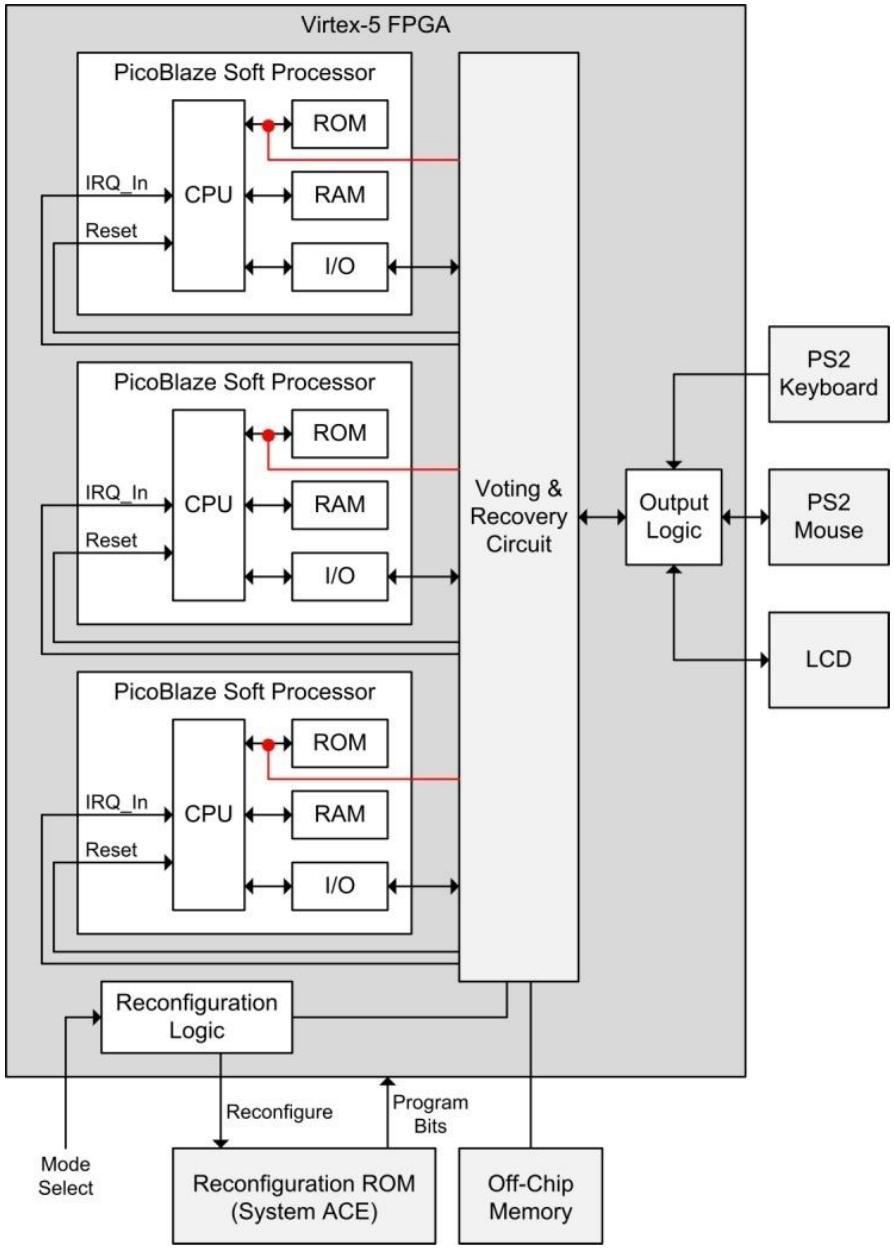
3) Radiation Tolerant Mode

- If **Radiation** is present

  - the FPGA can be configured with TMR on three processors

  - A voter is used to monitor for proper operation on memory interface

  - A recovery algorithm is used to resync and reinitialize the processors if the voter detects an error.



3) Radiation Tolerant Mode

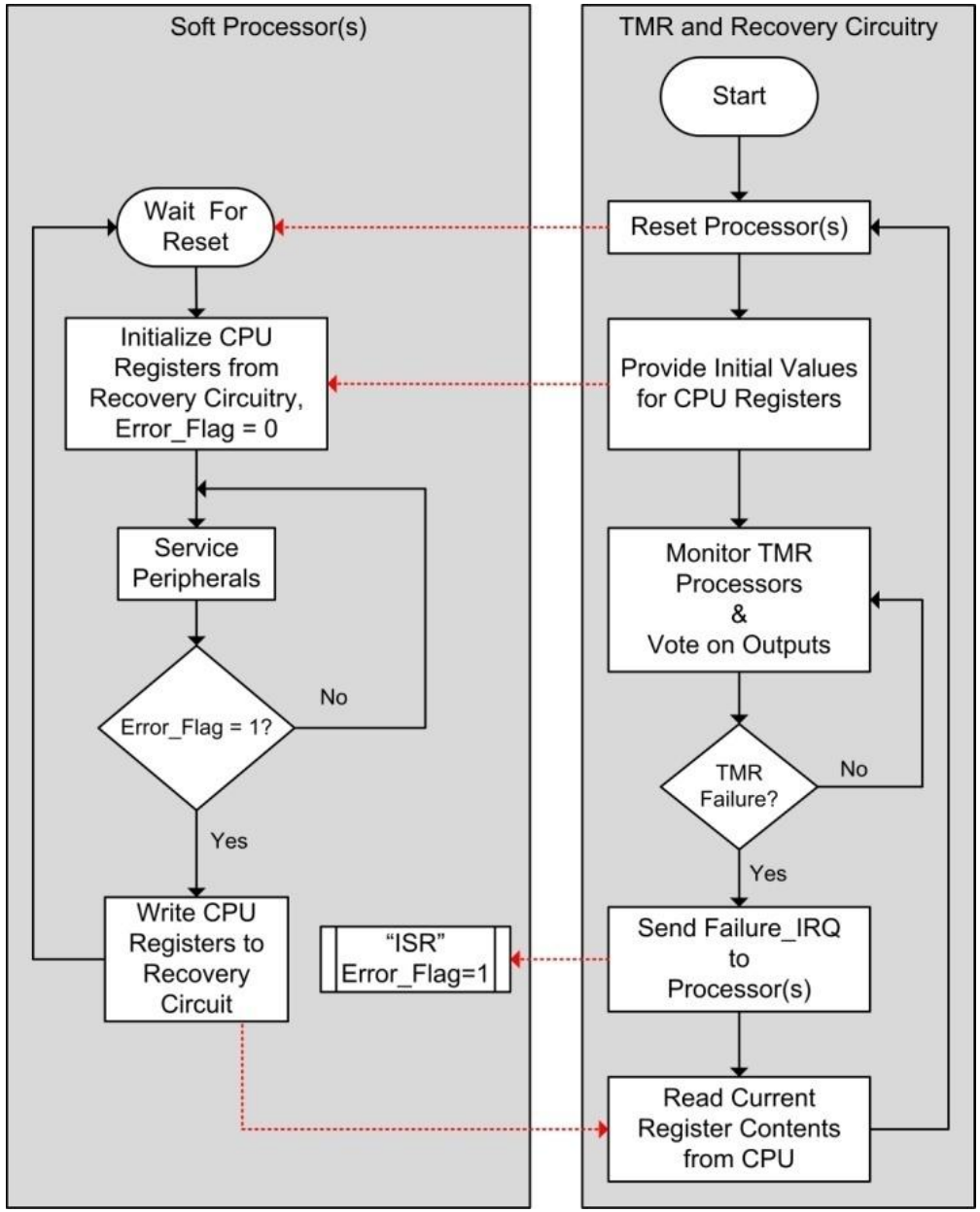
- Recovery Process

  - Upon error detection, the voter sets flag in processors using IRQ

  - after current task completion, the uP's off-load their variable information to rad-hard storage devices

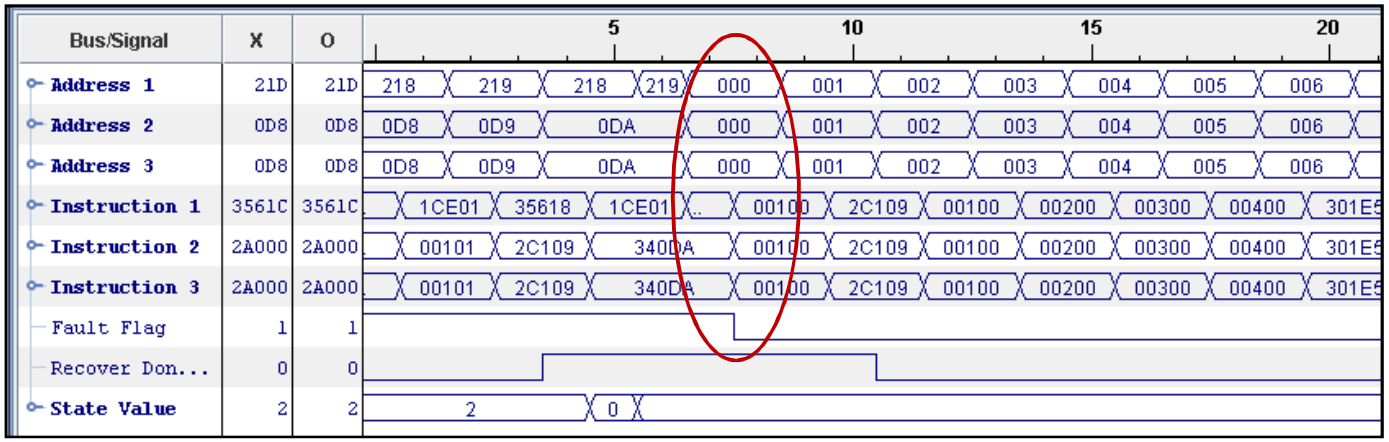
  - The TMR state machine then resets all processors

  - Upon start-up, each processors initializes its variables using data from rad-hard variable storage device

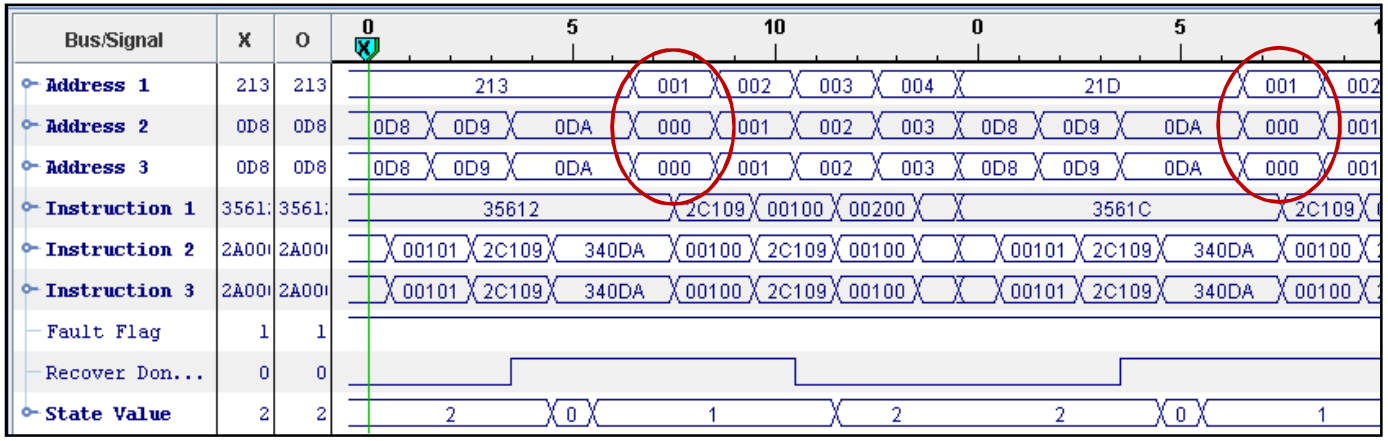


Chipscope View of Fault Recovery

- Single Fault



- Continuous Fault



Reconfiguration Process

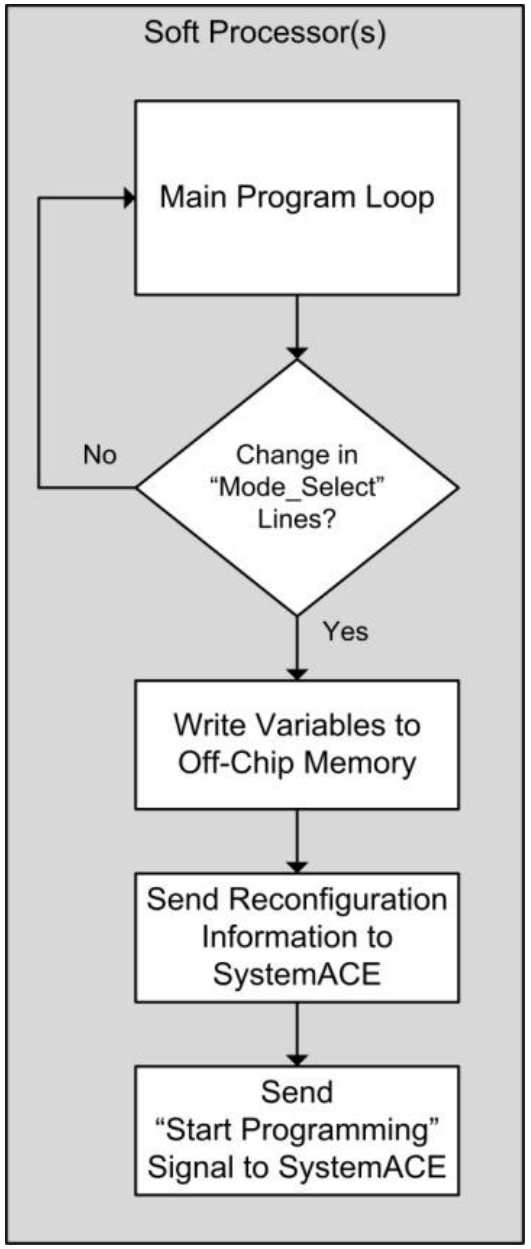
- Dynamic Reconfiguration Between Modes

  - Each design is stored in System ACE configuration memory

  - Each design monitors *radiation sensor* for a "change in mode" signal.

  - If reconfiguration is needed, each design off-loads its variable information to rad-hard storage device

  - Upon start-up, each design initializes its variables using data from rad-hard variable storage device



System Performance

- Timing Impact of Important System Events

System Event	Timing Dependencies	Total Time
Initial Power On	$t_{mouse} + t_{LCD} + t_{OCMW} + t_{sysace} + t_{OCMR}$	0.7ms + 1.67ms + 21.6ms + 504.0ms + 1.6ms = **529.6 ms**
Mode Config Change	$t_{OCMW} + t_{sysace} + t_{OCMR}$	21.6ms + 504.0ms + 1.6ms = **527.2ms**
Fault Recovery	$t_{OCMW} + t_{SMt} + t_{OCMR}$	21.6ms + 30.0ns+ 1.6ms = **23.2ms**

System Performance

- Area Usage for Three Configurations

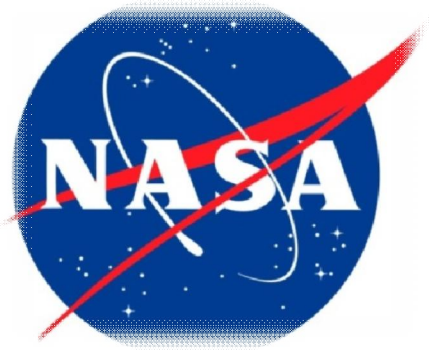
FPGA Resources	Resources Used		
	Parallel Processing	Low Power	Radiation Tolerant
Number of Slice Registers	261	102	355
Number of Slice LUTs	470	194	562
Number of occupied Slices	187	96	280
Number of LUT Flip Flop pairs	498	210	635

Ongoing Work

- *Microblaze* Implementation
- FPGA Partial Reconfiguration
- Scrubbing

Acknowledgements

- thank you to NASA and the Montana Space Grant Consortium for support of this work



Questions